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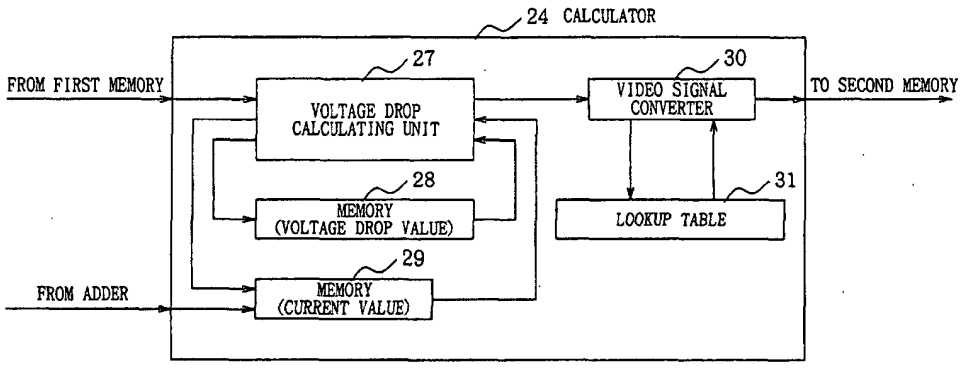
(54) PLANAR DISPLAY APPARATUS

(57) The invention provides a flat display device which comprises for pixels arranged along drive lines a voltage drop calculator 27 for calculating a voltage drop occurring in accordance with the position of each pixel, and a video signal converter 30 and a lookup table 31 for correcting the input signal to be supplied to the pixel in accordance with the magnitude of the calculated voltage drop, whereby crosstalk due to the voltage drop is prevented.

FIG. 2



EP 1 439 518 A1

Description

TECHNICAL FIELD

[0001] The present invention relates to flat display devices, such as organic electroluminescence display devices and inorganic electroluminescence display devices.

BACKGROUND ART

[0002] Progress has been made in recent years in developing flat displays of the self-luminescence type such as organic electroluminescence displays (hereinafter referred to as "organic EL displays") and inorganic electroluminescence displays (hereinafter referred to as "inorganic EL displays"). Use of organic EL displays, for example, in portable telephones is under study.

[0003] FIGS. 6 and 7 show an organic EL display, which is fabricated by forming an organic hole transport layer 15 and an organic electron transport layer 16 on opposite sides of an organic luminescent layer 14 to provide an organic layer 13 on a glass substrate 11 serving as a base, and forming anodes 12 and cathodes 17 on opposite sides of the organic layer 13. The organic luminescent layer 14 is caused to luminesce by applying a predetermined voltage across the anode 12 and the cathode 17.

[0004] The anodes 12 are made from transparent ITO (indium tin oxide), and the cathodes 17, for example, from an Al-Li alloy. The electrodes of each type are prepared in the form of stripes to intersect those of the other type in the form of a matrix. The anodes 12 are used as data electrodes, and the cathodes 17 as scanning electrodes. With one of horizontally extending scanning electrodes selected, voltage in accordance with input data is applied to data electrodes extending perpendicular to the scanning electrode, whereby the organic layer 13 is caused to luminesce at the intersections of the scanning electrode and the data electrodes to give a display of one line. The scanning electrodes are changed over one after another in the perpendicular direction to scan the matrix in the perpendicular direction to give a display of one frame.

[0005] The methods of driving such organic EL displays include the passive matrix driving method wherein the scanning electrodes and the data electrodes are used for time division driving, and the active matrix driving method wherein each pixel is held luminescent for one vertical scanning period.

[0006] On the other hand, FIGS. 10 and 11 show an inorganic EL display, which comprises a substrate 110 of glass or ceramic serving as a base, an inorganic layer 130 composed of an inorganic luminescent layer 140 and a dielectric layer 150 formed on one side of the layer 140, and first electrodes 120 and second electrodes 170 which are arranged respectively on opposite sides of the inorganic layer 130. A.C. Voltage is applied across the first electrode 120 and the second electrode 170 to cause the inorganic luminescent layer 140 to luminesce.

[0007] It is known that like organic EL displays of the passive matrix driving type, the inorganic EL display is adapted for time division driving using scanning electrodes and data electrodes. While the organic EL display is driven with direct current for passing current through the luminescent layer thereof, the inorganic EL display is driven with alternating current for passing current through the luminescent layer thereof.

[0008] In the organic EL display of the active matrix driving type, each organic EL element 20 providing one pixel 10 has a first transistor TR1 performing an on/off function, a second transistor TR2 for converting input data to a current value, and a capacitance element C performing a memory function as shown in FIG. 8. A drive line 4 is connected to the source of the second transistor TR2. A drive circuit 6 comprises a gate driver 61 for driving the scanning electrodes, and a source driver 62 for driving the data electrodes.

[0009] First, the gate driver 61 successively applies voltage to the scanning electrodes to bring the first transistors TR1 connected to the same scanning electrode into conduction. Data (input signal) is fed to the source driver 62 as timed with this scanning. Since the first transistor TR1 is in a conducting state at this time, the data is stored in the capacitance element C.

[0010] The operating state of the second transistor TR2 is dependent on the charge of data stored in the capacitance element C. For example, suppose the second transistor TR2 is brought into an operative state. Current is then supplied to the organic EL element 20 via the second transistor TR2. As a result, the EL element 20 luminesces. This luminescent state is maintained over one vertical scanning period.

[0011] The organic EL display 1 is self-luminescent as stated above, and the required pixels only need to be turned on, so that the display is adapted to reduce power consumption unlike the liquid crystal display wherein the backlight needs to be on at all times. This is also true with all flat displays of the self-luminescent type including inorganic EL displays.

[0012] For example, when white is displayed in a central area B of the screen of the organic EL display 1 shown in FIG. 9, with a given intermediate color presented in the area surrounding this area B, the upper and lower areas A and A' of drive lines (power supply lines) indicated in broken lines have luminance lower than the luminance corresponding to the input signal, unlike the left and right areas showing the intermediate color, hence the problem of so-called crosstalk. Although the central area B has luminance lower than the luminance corresponding to the input signal, the lower luminance is not conspicuous since there is nothing to be compared with the area.

[0013] Accordingly, an object of the present invention is to provide a flat display device which is suppressed in crosstalk.

DISCLOSURE OF THE INVENTION

[0014] The present applicant has clarified the cause for the above-mentioned crosstalk in flat display devices of the self-luminescent type. Although the cause involved in the organic EL display of the active matrix driving type will be described below, the cause for crosstalk will be similarly determined in organic EL displays and inorganic EL displays of the passive matrix driving type.

[0015] In the case where white is to be displayed in the area B within the screen of an organic EL display as shown in FIG. 9, great input voltage is applied to the gates of second transistors arranged in the area B, and great current is caused to correspondingly flow between the sources and drains of the second transistors from the drive lines 4.

[0016] The current supplied from a current source connected to one end of the drive line 4 dividedly flows into the second transistors TR2 of pixels 10 and is supplied to the transistors TR2 while flowing through the drive line 4 in one direction, so that the current value at the points of divisions is greatest at the division point in the most upstream position and smallest at the division point in the most downstream position. The current flowing through the drive line 4 is further influenced by electric resistance corresponding to the length of the drive line 4, and the electric resistance gives rise to a voltage drop.

[0017] Since the drive line needs to be supplied with current corresponding to the amount of luminescence to be produced as described above, the organic EL display has connected thereto a power source circuit or driver circuit for supplying current to the drive line. The power source circuit or driver circuit also involves output resistance, so that not only the voltage drop due to the resistance of the drive line but also a voltage drop due to the output resistance of the power source circuit or driver circuit occurs in accordance with the amount of luminescence.

[0018] In the example shown in FIG. 9, therefore, the voltage drop involved in each pixel is greatest in the area A, while the combined voltage drop is greatest in area A'. The term "combined voltage drop" means a voltage drop ΔV represented by Mathematical Expression 1 given later. In other words, the current supplied to the second transistor is smaller in the upstream area A and downstream area A' than in the area B, consequently failing to afford luminance corresponding to the input signal and generating crosstalk. A voltage drop occurs also in the area B, whereas since no adjacent image to be compared is present, a reduction in luminance does not appear obvious.

[0019] The present invention provides a flat display device wherein each of pixels comprises a luminescent layer and two electrodes arranged respectively on opposite sides of the luminescent layer, and a drive signal is supplied to each pixel from a drive circuit through a drive line to thereby apply a voltage in accordance with an input signal across the two electrodes and cause the luminescent layer to luminesce, the flat display device being characterized in that the display device comprises input signal correcting means for correcting the input signal in accordance with the magnitude of a voltage drop occurring in the drive signal to be supplied to the pixel. The luminescent layer is made from an organic material or inorganic material.

[0020] Stated specifically, the present invention provides a flat display device wherein a pair of electrodes are arranged respectively on opposite sides of a luminescent layer, and a voltage in accordance with an input signal is applied across the electrodes by a drive signal supplied through a drive line for each of pixels provided by the luminescent layer to cause the luminescent layer to luminesce, the flat display device being characterized in that the display device comprises:

means provided for the drive line for calculating a voltage drop occurring in the drive line in accordance with the position of the pixel, based on the input signal to be supplied to the pixel, and
means for correcting the input signal to be supplied to the pixel based on the magnitude of the calculated voltage drop.

[0021] With the flat display device of the invention described, the voltage drop occurring in the drive line in accordance with the position of each pixel is calculated, and the input signal to be supplied to the pixel is corrected based on the magnitude of the calculated voltage drop, so that the pixel is to luminesce with luminance according to the input signal.

[0022] When the display device is an organic EL display device of the active matrix driving type, the cathode is in the form of a sheet, and the anode is in the form of stripes. The pixels provided by an organic layer each have a first transistor TR1 to be brought into or out of conduction with the voltage of the cathode, a capacitance element C for storing a signal to be input from the anode by the first transistor conducting, and a second transistor TR2 for producing drive current in accordance with the input signal with a drive signal (electric power) to be supplied from the drive line.

[0023] Stated specifically, the voltage drop calculating means calculates the voltage drop based on the magnitude of current flowing through the pixel in accordance with the input signal and on a resistance value depending on the position of the pixel.

[0024] Further stated specifically, the voltage drop calculating means has a coefficient depending on the material characteristics of each of RGB pixels and calculates the magnitude of current flowing through the pixel in accordance with the coefficient and the input signal to the pixel.

[0025] Further stated specifically, the input signal correcting means comprises first conversion means for converting the magnitude of the calculated voltage drop

to a reduction in the current flowing through the pixel, and second conversion means for converting the current reduction obtained from the first conversion means to an amount of correction of the input signal to be supplied to the pixel.

[0026] Further stated specifically, the drive line is in the form of stripes extending in the same direction as the direction of scanning of display images.

[0027] With the flat display device of the present invention, each of pixels luminesces with luminance in accordance with the input signal despite a voltage drop occurring in the drive line. No crosstalk therefore occurs due to the voltage drop.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028]

FIG. 1 is a block diagram showing the construction of an organic EL display device according to the invention.

FIG. 2 is a block diagram showing the construction of a calculator.

FIG. 3 is a perspective view partly broken away and showing an organic EL display of the active matrix driving type for use in the invention.

FIG. 4 is a perspective view partly broken away and showing another organic EL display of the active matrix driving type for use in the invention.

FIG. 5 is an equivalent circuit diagram of a drive system for pixels.

FIG. 6 is a diagram showing the layered structure of an organic EL display of the passive matrix driving type.

FIG. 7 is a perspective view partly broken away and showing the organic EL display of the passive matrix driving type.

FIG. 8 is an equivalent circuit diagram of an organic EL display of the active matrix driving type.

FIG. 9 is a diagram for illustrating the problem of the organic EL display of the active matrix driving type.

FIG. 10 is a diagram showing the layered structure of an inorganic EL display of the passive matrix driving type.

FIG. 11 is a perspective view partly broken away and showing the inorganic EL display of the passive matrix driving type.

BEST MODE OF CARRYING OUT THE INVENTION

[0029] With reference to the drawings, a detailed description will be given of the invention as embodied into an organic EL display of the active matrix driving type. FIG. 1 shows an organic EL display device according to the invention which comprises an organic EL display 2 of the active matrix driving type, and a power source circuit 3 for supplying driving electric power to the display 2. The input signal to be given to the display 2 is fed to a correction circuit C shown in FIG. 1, thereby processed for correction as will be described below and thereafter supplied to the display 2.

[0030] Usable in the organic EL display 2 are an anode 12 in the form of stripes extending vertically of the screen as shown in FIG. 3, and a cathode 18 in the form of a sheet. Alternatively usable are an anode 12 in the form of stripes extending horizontally of the screen as shown in FIG. 4, and a cathode 18 in the form of a sheet. The present embodiment comprises an organic EL display 2 of the type shown in FIG. 4.

[0031] In the correction circuit C shown in FIG. 1, the input signal is first converted to digital data in an A/D converter 21, and thereafter fed to a first memory 22 and an adder 23. The input data is temporarily stored in (written to) the first memory 22, and upon lapse of one scanning period 1H, the data is output to (read by) a calculator 24 subsequently provided. The data is read and written at the same time for a delay of 1H. The adder 23 adds up the input data in an amount corresponding only to 1H, and delivers the sum to the subsequent calculator 24.

[0032] The calculator 24 performs the calculation to be described below based on the data input from the first memory 22 and the sum value input from the adder 23, whereby the input data is corrected in accordance with the magnitude of a voltage drop of the aforementioned drive line. The corrected data is temporarily stored in a second memory 25. The data is thereafter read from the second memory 25, converted to an analog signal in a D/A converter 26 and thereafter supplied to the organic EL display 2.

[0033] The principle of correction of data by the calculator 24 will now be described with reference to FIG. 5. Referring to FIG. 5, second transistors TR2 and organic EL elements 20 are connected in parallel to a drive line 4 extending horizontally for supplying electric power, the transistors, as well as the EL elements, being equal in number to the number n of pixels on one horizontal scanning line. A gradation voltage in accordance with the input data is applied to the gate of each second transistor TR2, and the current to be supplied to the organic EL element 20 from the drive line 4 via the second transistor TR2 is controlled according to the voltage.

[0034] Now suppose the points at each of which the drive line 4 branches off toward the second transistor are point 1 to point N as arranged downstream from the upstream side as illustrated, the resistance of the line from a point (contact portion) where the drive line 4 is connected to a current source (not shown) to the point 1 is R0, the electric resistance of each pixel to the current flowing therethrough is R, and the current flowing through the respective pixels are I1 to In. The voltage drops $\Delta V1$ to ΔVn at the respective points are expressed by Mathematical Expressions 1 given below.

(Mathematical Expressions 1)

$$\Delta V1 = (I1 + I2 + I3 + \ldots I_{n-1} + In) \times R0$$
$$+ \underline{(I1 + I2 + I3 + \ldots I_{n-1} + In) \times R}$$
$$\Delta V2 = (I1 + I2 + I3 + \ldots I_{n-1} + In) \times R0$$
$$+ (I1 + I2 + I3 + \ldots I_{n-1} + In) \times R$$
$$+ \underline{(I2 + I3 + \ldots I_{n-1} + In) \times R}$$
$$\Delta V3 = (I1 + I2 + I3 + \ldots I_{n-1} + In) \times R0$$
$$+ (I1 + I2 + I3 + \ldots I_{n-1} + In) \times R$$
$$+ (I2 + I3 + \ldots I_{n-1} + In) \times R$$
$$+ \underline{(I3 + \ldots I_{n-1} + In) \times R}$$
$$.$$
$$.$$
$$\Delta V_{n-1} = (I1 + I2 + I3 + \ldots I_{n-1} + In) \times R0$$
$$+ (I1 + I2 + I3 + \ldots I_{n-1} + In) \times R$$
$$+ (I2 + I3 + \ldots I_{n-1} + In) \times R$$
$$+ (I3 + \ldots I_{n-1} + In) \times R$$
$$.$$
$$.$$
$$+ \underline{(I_{n-1} + In) \times R}$$
$$\Delta V_n = (I1 + I2 + I3 + \ldots I_{n-1} + In) \times R0$$
$$+ (I1 + I2 + I3 + \ldots I_{n-1} + In) \times R$$
$$+ (I2 + I3 + \ldots I_{n-1} + In) \times R$$
$$+ (I3 + \ldots I_{n-1} + In) \times R$$
$$.$$
$$.$$
$$+ (I_{n-1} + In) \times R$$
$$+ \underline{In \times R}$$

[0035] With reference to Mathematical Expressions 1 given above, the underlined term included in the voltage drop expression at a particular point is a term added to the expression of the voltage drop at the point immediately preceding the particular point. By adding a voltage corresponding to the voltage drop of Mathematical Expression 1 to the gradation voltage to be applied to the gate of the second transistor TR2 concerned, the desired current value, namely, luminescence of desired luminance, is available free of the influence of the voltage drop.

[0036] Suppose the voltage drop due to the resistance R0 is A, and the sum of the currents I1 to In flowing through the pixels is I. Expressions 1 can then be rewritten as Mathematical Expressions 2 given below by replacing the voltage drop expression at each point with a voltage drop expression at the immediately preceding point.

(Mathematical Expressions 2)

$$\Delta V1 = A + \underline{I \times R}$$
$$\Delta V2 = \Delta V1 + \underline{(\text{current value at point 1} - I1) \times R}$$
$$\Delta V3 = \Delta V2 + \underline{(\text{current value at point 2} - I2) \times R}$$
$$.$$
$$.$$
$$\Delta V_{n-1} = \Delta V_{n-2} + \underline{(\text{current value at point n-2} - I_{n-2}) \times R}$$
$$\Delta V_n = \Delta V_{n-1} + \underline{(\text{current value at point n-1} - I_{n-1}) \times R}$$

[0037] Accordingly, the specific arrangement shown in FIG. 2 is used as the calculator 24 shown in FIG. 1. With reference to FIG. 2, the data to be input from the first memory 22 is fed to a voltage drop calculating unit 27, and the data to be input from the adder 23 is stored in a fourth memory 29. The unit 27 calculates the voltage drop value and the current value at the contemplated point for which the calculations are to be made, based on the voltage drop value and the current value at the point immediately preceding the contemplated point. The calculated voltage drop value and the current value are stored in a third memory 28 and the fourth memory 29, respectively.

[0038] The voltage drop calculating unit 27 first calculates the voltage drop value $\Delta V1$ and current value at point 1 based on the data (current value I) stored in the fourth memory 29, and feeds the results to the third memory 28 and the fourth memory 29, respectively. Subsequently, based on the voltage drop value $\Delta V1$ at point 1 stored in the third memory 28 and the current value at point 1 stored in the fourth memory 29, the unit 27 calculates the voltage drop value $\Delta V2$ and current value at point 2, and supplies the results to the third memory 28 and the fourth memory 29, respectively. In this way, the voltage drop values and the current values at the respective points are successively calculated, with the result that the voltage drop values at all points

are obtained.

[0039] The voltage drop values obtained at the respective points by the voltage drop calculating unit 27 are fed to a video signal converter 30, which has connected thereto a lookup table 31. By reference to the lookup table 31, the video signal converter 30 converts the voltage drop value from the calculating unit 27 to a signal. Defined in the lookup table 31 are the source-drain voltage-current relationship and the relationship between the base voltage and the source-drain current, as determined for each second transistor TR2.

[0040] By reference to the lookup table 31, the video signal converter 30 converts the voltage drop value at each point to a current reduction of the second transistor TR2 and further to an increase in base voltage required to compensate for the current reduction, adds the result to the initial input data obtained from the first memory for the correction of the data, and output the corrected data to the second memory 25. In the case where the relationship involved in the conversion by the video signal converter 30 is a linear relationship or can be expressed by a functional equation, the signal conversion with use of the lookup table 31 can be replaced by processing for the multiplication of a constant or calculation with use of the functional equation.

[0041] Furthermore, the power source circuit 3 of FIG. 1 involves output resistance, which gives rise to the same phenomenon as the voltage drop due to the wiring resistance of the drive line described. Accordingly, such a voltage drop can be corrected by the same method as the voltage drop due to the wiring resistance of the drive line.

[0042] In the case of the organic EL display device of the present invention described, the input signal to each pixel is corrected in accordance with the voltage drop occurring in the drive line and the voltage drop occurring in the power source circuit 3. The pixel can therefore be caused to luminesce with luminance corresponding to the input signal despite the voltage drop, and is rendered free of the crosstalk that would otherwise result from the voltage drop. Further because the drive line 4 is disposed along the horizontal scanning lines, the correction processing described can be effected for every horizontal scanning line. This ensures facilitated calculation processing.

[0043] The device of the present invention is not limited to the foregoing embodiment in construction but can be modified variously without departing from the technical scope defined in the appended claims. For example, the present invention can be embodied not only into organic EL displays of the active matrix driving type but also into organic EL displays of the passive matrix driving type or inorganic EL displays of the passive matrix driving type.

Claims

1. A flat display device wherein each of pixels comprises a luminescent layer and two electrodes arranged respectively on opposite sides of the luminescent layer, and a drive signal is supplied to each pixel from a drive circuit through a drive line to thereby apply a voltage in accordance with an input signal across the two electrodes and cause the luminescent layer to luminesce, the flat display device being **characterized in that** the display device comprises input signal correcting means for correcting the input signal in accordance with the magnitude of a voltage drop occurring in the drive signal to be supplied to the pixel.

2. A flat display device according to claim 1 wherein the input signal correcting means comprises means for calculating a reduction in the amount of luminescence occurring in accordance with the position of the pixel, and corrects the input signal based on the result of calculation.

3. A flat display device according to claim 1 wherein the input signal correcting means comprises means for producing an input signal corrected in accordance with the input signal to be supplied to the pixel and the position of the pixel.

4. A flat display device according to claim 1 wherein the input signal correcting means compensates the input signal to the pixel for the voltage drop occurring in the drive line, in accordance with the position of the pixel.

5. A flat display device according to claim 1 wherein the input signal correcting means compensates the input signal to the pixel for the voltage drop occurring in the drive circuit for supplying the drive signal to the drive line.

6. A flat display device according to any one of claims 1 to 5 wherein the luminescent layer comprises an organic material.

7. A flat display device according to any one of claims 1 to 5 wherein the luminescent layer comprises an inorganic material.

8. A flat display device wherein a pair of electrodes are arranged respectively on opposite sides of a luminescent layer, and a voltage in accordance with an input signal is applied across the electrodes by a drive signal supplied through a drive line for each of pixels provided by the luminescent layer to cause the luminescent layer to luminesce, the flat display device being **characterized in that** the display device comprises:

means provided for the drive line for calculating a voltage drop occurring in the drive line in accordance with the position of the pixel, based on the input signal to be supplied to the pixel, and

means for correcting the input signal to be supplied to the pixel based on the magnitude of the calculated voltage drop.

9. A flat display device according to claim 8 wherein the luminescent layer comprises an organic material.

10. A flat display device according to claim 8 wherein the luminescent layer comprises an inorganic material.

11. A flat display device according to any one of claims 8 to 10 which is of the active matrix driving type and wherein the cathode is in the form of a sheet, and the anode is in the form of stripes.

12. A flat display device according to any one of claims 8 to 10 which is of the passive matrix driving type and wherein one of the electrodes is in the form of stripes extending horizontally, and the other electrode is in the form of stripes extending vertically.

13. A flat display device according to any one of claims 8 to 12 wherein the drive lines are in the form of stripes extending in the same direction as the direction of scanning of display images.

14. A flat display device according to any one of claims 8 to 13 wherein the voltage drop calculating means calculates the voltage drop based on the magnitude of current flowing through the pixel in accordance with the input signal and on a resistance value depending on the position of the pixel.

15. A flat display device according to any one of claims 8 to 13 wherein the voltage drop calculating means has a coefficient depending on the material characteristics of each of RGB pixels and calculates the magnitude of current flowing through the pixel in accordance with the coefficient and the input signal to the pixel.

16. A flat display device according to any one of claims 8 to 15 wherein the input signal correcting means comprises first conversion means for converting the magnitude of the calculated voltage drop to a reduction in the current flowing through the pixel, and second conversion means for converting the current reduction obtained from the first conversion means to an amount of correction of the input signal to be supplied to the pixel.

FIG. 1

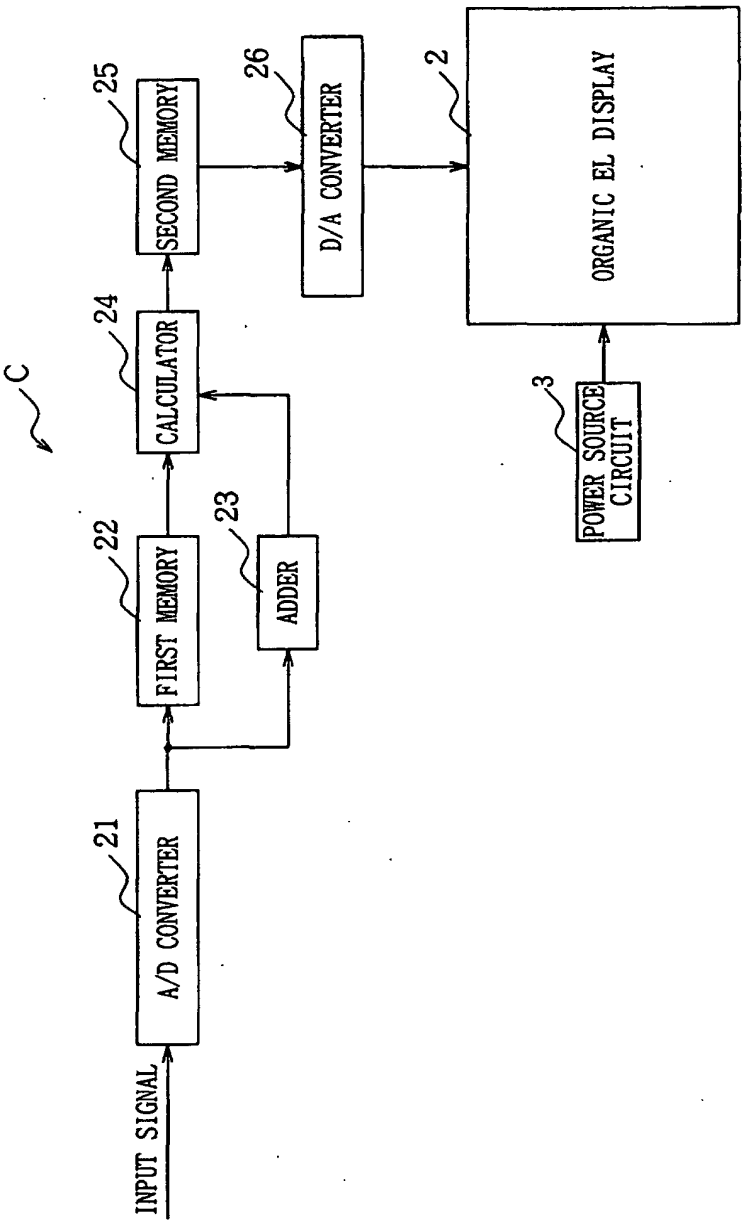

C
INPUT SIGNAL
21
A/D CONVERTER
22
FIRST MEMORY
23
ADDER
24
CALCULATOR
25
SECOND MEMORY
26
D/A CONVERTER
2
ORGANIC EL DISPLAY
3
POWER SOURCE CIRCUIT

FIG. 2

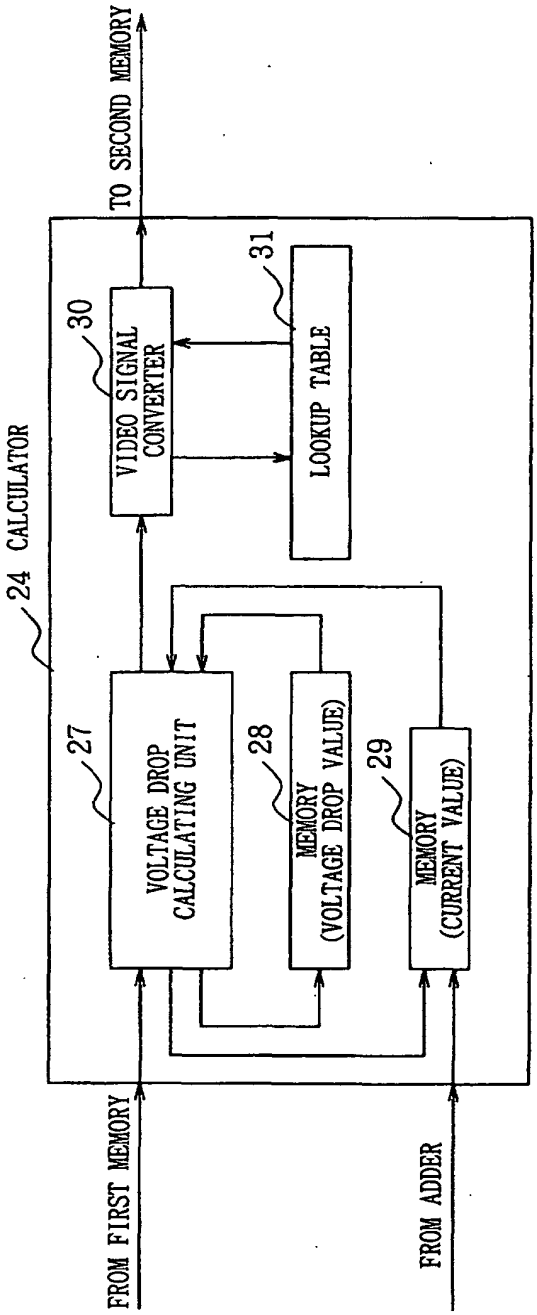

TO SECOND MEMORY
24 CALCULATOR
30
VIDEO SIGNAL CONVERTER
31
LOOKUP TABLE
27
VOLTAGE DROP CALCULATING UNIT
28
MEMORY (VOLTAGE DROP VALUE)
29
MEMORY (CURRENT VALUE)
FROM FIRST MEMORY
FROM ADDER

FIG. 3

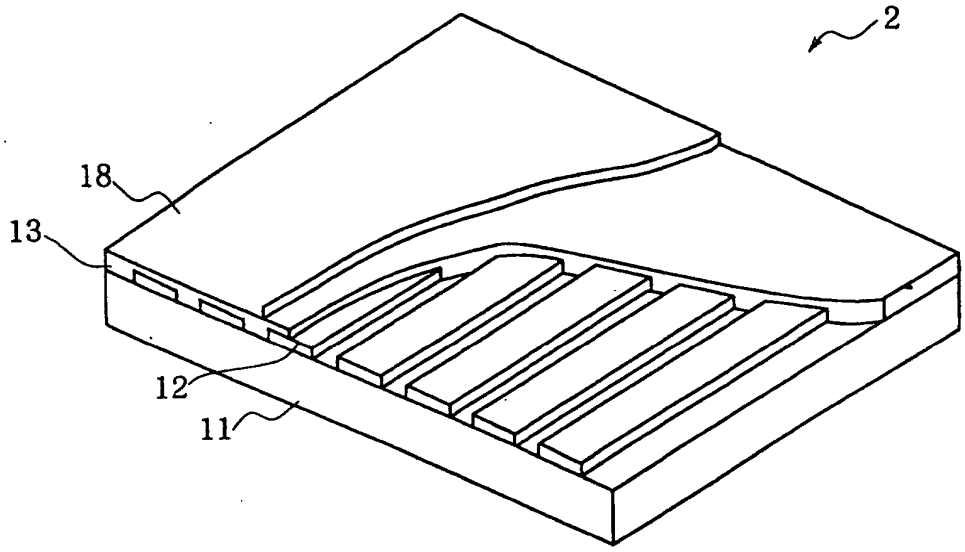


FIG. 4

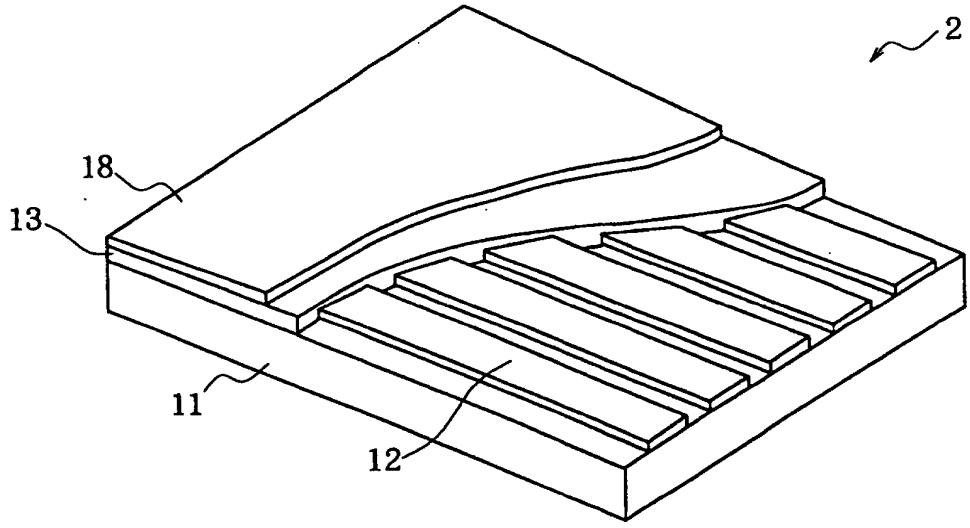


FIG. 5

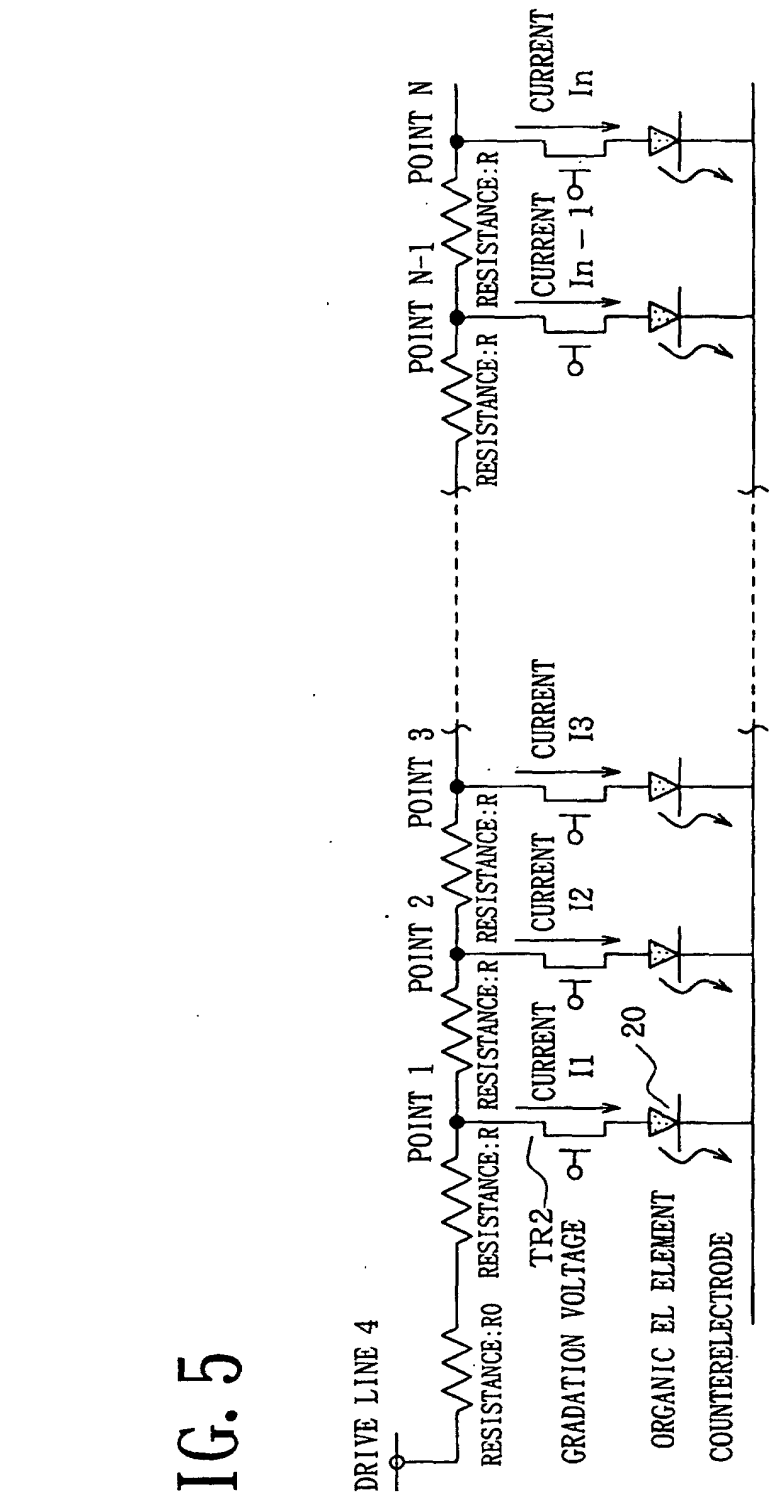

DRIVE LINE 4
RESISTANCE:R0
POINT 1
RESISTANCE:R
POINT 2
RESISTANCE:R
POINT 3
RESISTANCE:R
POINT N-1
RESISTANCE:R
POINT N
TR2
GRADATION VOLTAGE
CURRENT I1
CURRENT I2
CURRENT I3
CURRENT In - 1
CURRENT In
20
ORGANIC EL ELEMENT
COUNTERELECTRODE

FIG. 6

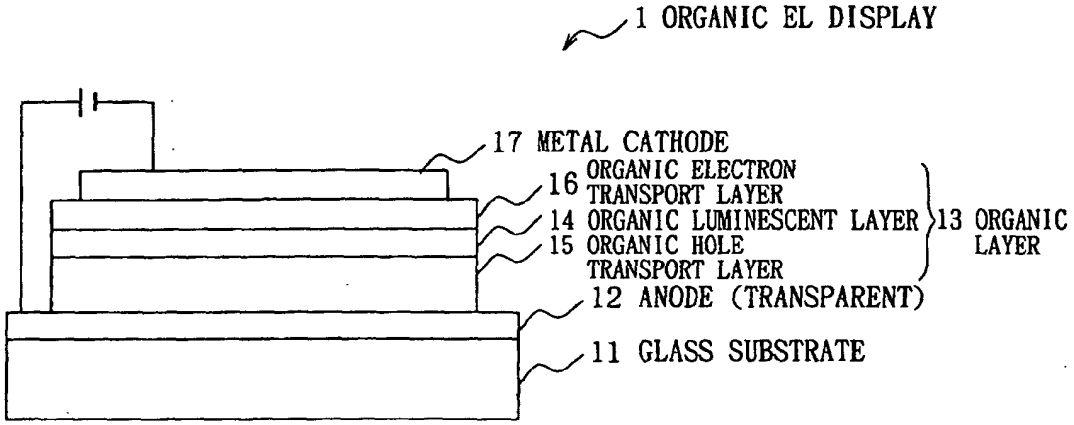

1 ORGANIC EL DISPLAY
17 METAL CATHODE
16 ORGANIC ELECTRON TRANSPORT LAYER
14 ORGANIC LUMINESCENT LAYER
15 ORGANIC HOLE TRANSPORT LAYER
13 ORGANIC LAYER
12 ANODE (TRANSPARENT)
11 GLASS SUBSTRATE

FIG. 7

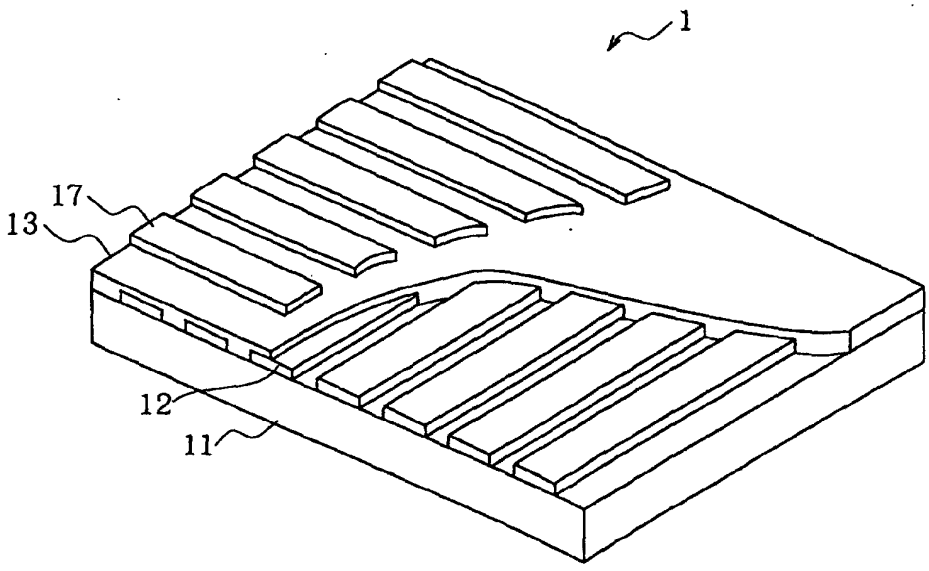

1
17
13
12
11

FIG. 8

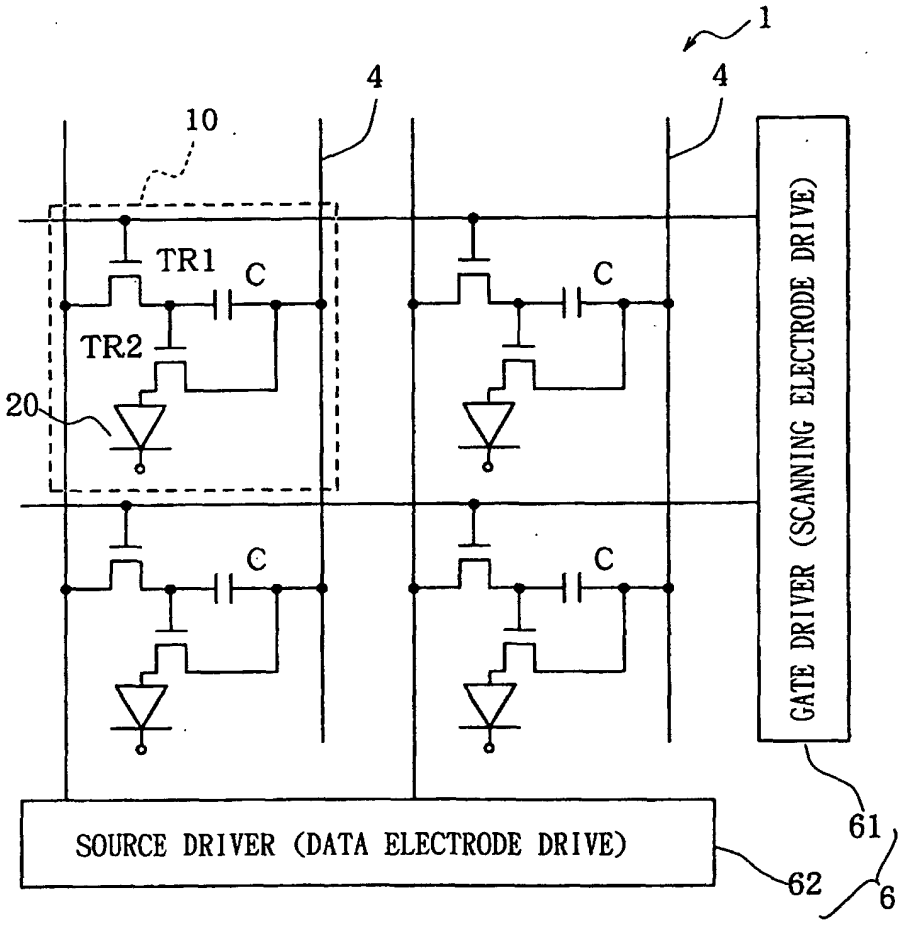

1
4
4
10
TR1
C
TR2
20
C
C
C
GATE DRIVER (SCANNING ELECTRODE DRIVE)
61
SOURCE DRIVER (DATA ELECTRODE DRIVE)
62
6

FIG. 9

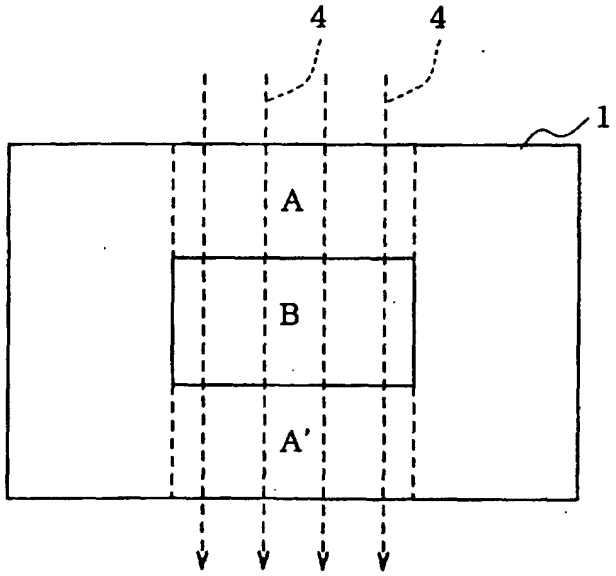


FIG. 10

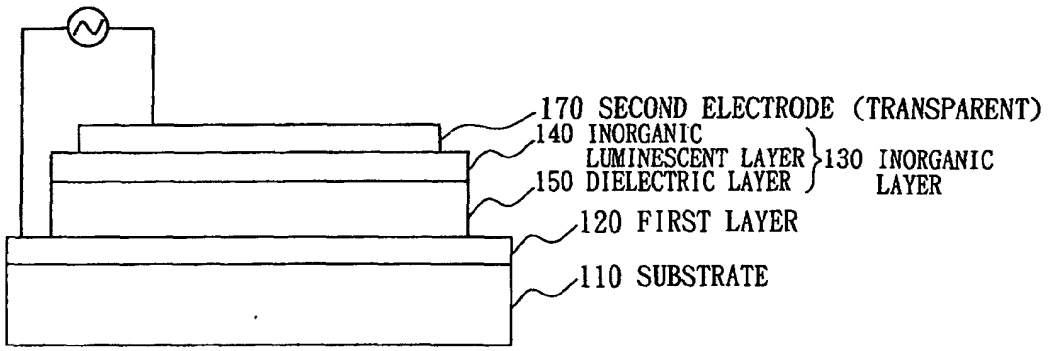
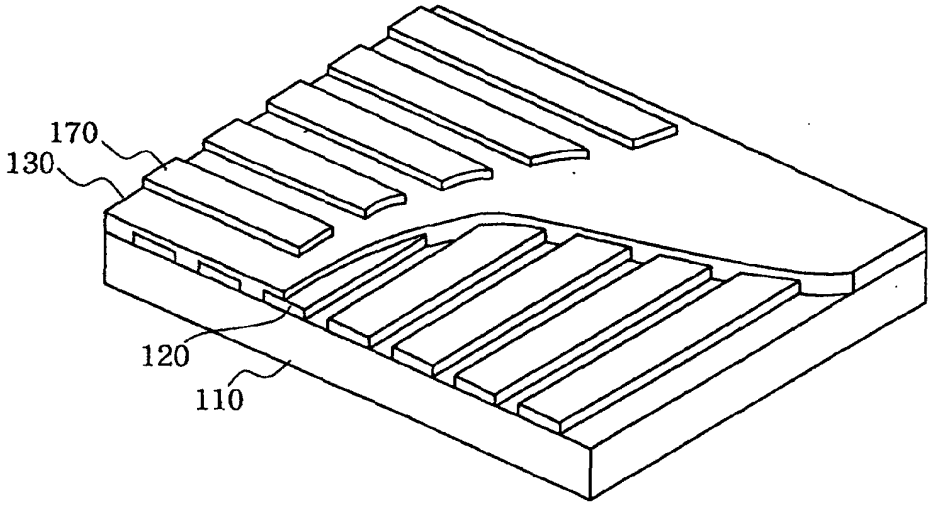

170 SECOND ELECTRODE (TRANSPARENT)
140 INORGANIC LUMINESCENT LAYER
150 DIELECTRIC LAYER
130 INORGANIC LAYER
120 FIRST LAYER
110 SUBSTRATE

FIG. 11


170
130
120
110

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP02/09922

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] G09G3/30, 3/20, H05B33/12

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] G09G3/30, 3/20, H05B33/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1926-1996	Jitsuyo Shinan Toroku Koho	1996-2002
Kokai Jitsuyo Shinan Koho	1971-2002	Toroku Jitsuyo Shinan Koho	1994-2002

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 8-248920 A (Canon Inc.), 27 September, 1996 (27.09.96), Full text; all drawings & EP 0686993 A1 & US 5734361 A	1-16
Y	JP 2000-242208 A (Canon Inc.), 08 September, 2000 (08.09.00), Par. No. [0238] (Family: none)	1-16
Y	JP 2001-109398 A (Sanyo Electric Co., Ltd.), 20 April, 2001 (20.04.01), Full text; all drawings (Family: none)	1-6,8-9,11, 13-16

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"P" document published prior to the international filing date but later than the priority date claimed
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 October, 2002 (29.10.02)	19 November, 2002 (19.11.02)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP02/09922

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 11-338413 A (Canon Inc.), 10 December, 1999 (10.12.99), Par. Nos. [0051] to [0079]; Figs. 1 to 6 (Family: none)	5
A	JP 61-83596 A (Sharp Corp.), 28 April, 1986 (28.04.86), Full text; all drawings & GB 2165078 A & DE 3534350 A1 & US 4686426 A & US 4983885 A	5
Y	JP 10-112391 A (Mitsubishi Electric Corp.), 28 April, 1998 (28.04.98), Full text; all drawings (Family: none)	6,9,11
Y	JP 7-295509 A (Tec Co., Ltd.), 10 November, 1995 (10.11.95), Full text; all drawings (Family: none)	7,10-11
A	JP 9-115673 A (Sony Corp.), 02 May, 1997 (02.05.97), Full text; all drawings & US 5886474 A & US 6177767 A	1-16
A	JP 3-189621 A (Seiko Epson Corp.), 19 August, 1991 (19.08.91), Full text; all drawings & EP 0434033 A2	1-16

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